DETAILED ACTION

Response to Arguments

1. The amendment filed on 06/23/2010 is acknowledged and entered by the examiner.

Claim Status

2. Claims 21, 23-25, 29, 32, 34, 36-39 and 41-46 are currently pending in the instant application. Claims 1-20, 22, 26-28, 30, 31, 33, 35, 40 and 47 have been canceled.

Reasons for Allowance

3. Claims 21, 23-25, 29, 32, 34, 36-39 and 41-46 allowed over the prior art record.

4. The following is an examiner's statement of reasons for allowance:

The applicant's remarks, filed on 06/23/2010, have been carefully reviewed with updated search. Consequently, reasons for allowance of claims 21, 23-25, 29, 32, 34, 36-39 and 41-46 are set forth in according with the following:

Westergren et al. (U.S PAT. 5,423,076) teaches a transceiver which operates in separate transmit and receive bands has a first conversion stage for generating a first IF signal translation of a receive signal, which first conversion stage also functions as a first and final, hence, single conversion stage for generating a transmit signal at its

transmission frequency. A modulated transmit signal component used in the single conversion to the transmission frequency of the transmission signal has harmonics which lie outside the transmission band and is of a frequency which permits a substantial overlap of transmit and receive injection frequencies generated by a first numerically controlled signal generator which are applied to a first mixer of the first conversion stage during respective transmit and receive mode operations.

Watanabe (U.S PAT. 5,319,798) teaches a radio transceiver including a pahe lock loop (PLL) synthesizer and is adaptable to a TDMA system in which the frequency of a radio frequency carrier is switched frequently at high speed. When an unlock alarm of the PLL synthesizer is used as one of the device alarms, the unlock alarm to be generated in an initial unlock period which is usually provided every switching of an output frequency of the PLL synthesizer is not used as one of the device alarms. The prohibition of generation of this unlock alarm is started in synchronism with a frequency control signal supplied from a control portion of the radio transceiver to a frequency divider of the PLL synthesizer for switching the carrier frequency and is limited to an OFF period of the carrier transmitting/receiving period.

Consider claims 21, 23, 24 and 29, the prior arts made of record, alone or in combination, fails to clearly teach or fairly suggest a transceiver comprising: a digital synthesizer; and a phase locked loop coupled to the digital synthesizer; wherein when the transceiver is in a transmitting mode, the digital synthesizer is configured to receive a modulation signal, modulate a reference signal in response to the modulation signal, and transmit the modulated reference signal to the phase locked loop; wherein when

the transceiver is in a receiving mode, the digital synthesizer is configured to receive a non-modulation signal, generate a non-modulated reference signal, and transmit the non-modulated reference signal to the phase locked loop; and wherein the digital synthesizer and the phase locked loop form a digital synthesizer-driven phase locked loop, and the digital synthesizer driven phase locked loop is configured to operate in a modulating state when the transceiver is in the transmitting mode and is configured to operate in an oscillating state when the transceiver is in the receiving mode, as specified in the independent claim 21, and further limitations of their respective dependent claims 23, 24 and 29.

Consider claim 25, the prior arts made of record, alone or in combination, fails to clearly teach or fairly suggest a transceiver comprising: a digital synthesizer; a phase locked loop; a modulation signal generator configured to transmit a modulation signal to the digital synthesizer in response to a first control signal; and a non-modulation signal generator configured to transmit a non-modulation signal to the digital synthesizer in response to a second control signal; wherein in response to receiving the modulation signal, the digital synthesizer is configured to modulate a reference signal by the modulation signal and to transmit the modulated reference signal to the phase locked loop; wherein in response to receiving the non-modulation signal, the digital synthesizer is configured to generate a non-modulated reference signal and to transmit the non-modulated reference signal to the phase locked loop; wherein the first control signal is generated when the transceiver is in a transmitting mode and the second control signal is generated when the transceiver is in a receiving mode; and wherein the digital

synthesizer and the phase locked loop form a digital synthesizer-driven phase locked loop, and the digital synthesizer driven phase locked loop is configured to operate in a modulating state when the transceiver is in the transmitting mode and is configured to operate in an oscillating state when the transceiver is in the receiving mode, as specified in the independent claim 25.

Consider claims 32, the prior arts made of record, alone or in combination, fails to clearly teach or fairly suggest a unit comprising: a transceiver comprising, a digital synthesizer, and a phase locked loop; wherein when the transceiver is in a transmitting mode, the digital synthesizer ks configured to receive a modulation signal, modulate a reference signal in response to the modulation signal, and transmit the modulated reference signal to the phase locked loop; wherein when the transceiver is in a receiving mode, the digital synthesizer is configured to receive a non-modulation signal, generate a non-modulated reference signal, and transmit the non-modulated reference signal to the phase locked loop; and wherein the digital synthesizer and the phase locked loop form a digital synthesizer-driven phase locked loop, and the digital synthesizer-driven phase locked loop is configured to operate in a modulating state when the transceiver is in the transmitting mode and is configured to operate in an oscillating state when the transceiver is in the receiving mode, as specified in the independent claim 32.

Consider claims 34 and 36-38, the prior arts made of record, alone or in combination, fails to clearly teach or fairly suggest a method of transmitting signals, the method comprising: transmitting a modulation signal to a digital synthesizer of a transceiver when the transceiver is in a transmitting mode; transmitting a non-

modulation signal to the digital synthesizer when the transceiver is in a receiving mode; in response to receiving the modulation signal, modulating by the digital synthesizer a reference signal by the modulation signal and transmitting the modulated reference signal to a phase locked loop of the transceiver; in response to receiving the non-modulation signal, generating by the digital synthesizer a non-modulated reference signal and transmitting the non-modulated reference signal to the phase locked loop; operating the digital synthesizer and the phase locked loop as a digital synthesizer-driven phase locked loop; operating the digital synthesizer-driven phase locked loop in a modulating state when the transceiver is in the transmitting mode; and operating the digital synthesizer-driven phase locked loop in an oscillating state when the transceiver is in the receiving mode, as specified in the independent claim 34, and further limitations of their respective dependent claims 36-38.

Consider claims 39 and 41-43, the prior arts made of record, alone or in combination, fails to clearly teach or fairly suggest a method of transmitting signals, the method comprising: in response to receiving a modulation signal, modulating by a digital synthesizer of a transceiver a reference signal by a modulation signal and transmitting the modulated reference signal to a phase locked loop of the transceiver; in response to receiving a non-modulation signal, generating by the digital synthesizer a non-modulated reference signal and transmitting the non-modulated reference signal to the phase locked loop; operating the digital synthesizer and the phase locked loop as a digital synthesizer-driven phase locked loop; operating the digital synthesizer-driven phase locked loop in a modulating state when the transceiver is in a transmitting mode;

and operating the digital synthesizer-driven phase locked loop in an oscillating state when the transceiver is in a receiving mode; wherein the modulation signal is transmitted to the digital synthesizer by a modulation signal generator when the transceiver is in the transmitting mode, and wherein the non-modulation signal is transmitted to the digital synthesizer by a non-modulation signal generator when the transceiver is in the receiving mode, as specified in the independent claim 39, and further limitations of their respective dependent claims 41-43.

Consider claims 44-46, the prior arts made of record, alone or in combination, fails to clearly teach or fairly suggest a method of transmitting signals, the method comprising: in response to receiving a first control signal, transmitting a modulation signal to a digital synthesizer of a transceiver; in response to receiving a second control signal, transmitting a non-modulation signal to the digital synthesizer; operating the digital synthesizer and the phase locked loop as a digital synthesizer-driven phase locked loop; operating the digital synthesizer-driven phase locked loop in a modulating state when the transceiver is in a transmitting mode; and operating the digital synthesizer-driven phase locked loop in an oscillating state when the transceiver is in a receiving mode; wherein the first control signal is generated when the transceiver is in the transmitting mode and the second control signal is generated when the transceiver is in the receiving mode, as specified in the independent claim 44, and further limitations of their respective dependent claims 45 and 46.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

Hand-delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571) 272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan H. Nguyen/
Examiner
Art Unit 2618